Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1 (original): A phase-frequency detector for adjusting a target clock signal and an input signal to the same phase comprising:

a first logic gate for receiving a first protection signal and a second protection signal, and for outputting a third protection signal according to a result of a corresponding logic arithmetic;

a first flip-flop electrically connected to the first logic gate, the first flip-flop for receiving the third protection signal, and for outputting the third protection signal as a first output signal when triggered by the target clock signal;

a second flip-flop electrically connected to the first logic gate, the second flip-flop for receiving the third protection signal, and for outputting the third protection signal as a second output signal when triggered by the input signal;

a second logic gate electrically connected to the first flip-flop and the second flip-flop, the second logic gate for receiving the first output signal and the second output signal, and for outputting a fourth protection signal according to a result of a corresponding logic arithmetic; and

a third logic gate electrically connected to the second logic gate, the third logic gate for receiving the third protection signal and the fourth protection signal, and for outputting a fifth protection signal according to a result of a corresponding logic arithmetic;

wherein a logic level of the fifth protection signal is used to determine whether to compare the phase of the input signal and the phase of the target clock signal.

2 (original): The phase-frequency detector of claim 1, wherein each of the first logic gate, the second logic gate, and the third logic gate is an OR gate.

3 (original): The phase-frequency detector of claim 1, wherein the first flip-flop and the second flip-flop are both D-type flip-flops.

4 (original): The phase-frequency detector of claim 1, wherein the first flip-flop and the second flip-flop are both falling-edge-triggered D-type flip-flops.

5 (original): The phase-frequency detector of claim 1 further comprising:

a control signal generator connected the target clock signal, the input signal and the fifth protection signal, the control signal generator for determining whether or not to compare the phase of the input signal and the phase of the target clock signal according to the logic level of the fifth protection signal.

6 (original): The phase-frequency detector of claim 5, wherein when the fifth protection signal corresponds to a first logic level, the control signal generator determines to stop the comparison of the phase of the input signal and the phase of the target clock signal.

7 (original): The phase-frequency detector of claim 5, wherein when the fifth protection signal corresponds to a second logic level, the control signal generator determines to compare the phase of the input signal with the phase of the target clock signal to output a voltage control signal for adjusting the target clock signal and the input signal to the same phase.

8 (currently amended): The phase-frequency detector of claim 1, further comprising:

a first inverter electrically connected to a triggered end of the first flip-flop, the first inverter for inverting the target clock signal before the target clock signal is inputted to the triggered end of the ~~second~~ first flip-flop;

a second inverter electrically connected to a triggered end of the second flip-flop, the second inverter for inverting the input signal before the input signal is inputted to the triggered end of the second flip-flop.

9 (original): The phase-frequency detector of claim 1, wherein the phase-frequency detector is utilized in an optical disc system.

10 (original): The phase-frequency detector of claim 8, wherein the input signal is a wobble signal of an optical disc, and the target clock signal is a wobble clock signal corresponding to the wobble signal in the optical disc system.

11 (original): A phase-frequency detecting method for adjusting a target clock signal synchronous to an input signal, the phase-frequency detecting method comprising:

executing a first logic arithmetic on a first protection signal and a second protection signal for outputting a third protection signal;

outputting the third protection signal to form a first output signal when triggered by the target clock signal;

outputting the third protection signal to form a second output signal when triggered by the input signal;

executing a second logic arithmetic on the first output signal and the second output signal for outputting a fourth protection signal;

executing a third logic arithmetic on the third protection signal and the fourth protection signal for outputting a fifth protection signal; and

determining whether or not to compare the phase of the input signal and the phase of the target clock signal according to a logic level of the fifth protection signal.

12 (original): The phase-frequency detecting method of claim 11, wherein the step of determining whether or not to compare the phase of the input signal and the phase of

the target clock signal further comprises:

stopping the comparison of the phase of the input signal and the phase of the target clock signal, when the fifth protection signal corresponds to a first logic signal.

13 (original): The phase-frequency detecting method of claim 11, wherein the step of determining whether or not to compare the phase of the input signal and the phase of the target clock signal further comprises:

comparing the phase of the input signal with the phase of the target clock signal; and

outputting a voltage control signal for adjusting the target clock signal to the same phase as the input signal, when the fifth protection signal corresponds to a second logic level.

14 (original): The phase-frequency detecting method of claim 13, wherein the step of outputting the third protection signal to form a first output signal further comprises:

outputting the third protection signal to form the first output signal, when the target clock signal has a transition from a high logic level to a low logic level.

15 (original): The phase-frequency detecting method of claim 13, wherein the step of outputting the third protection signal to form a second output signal further comprises:

outputting the third protection signal to form the second output signal, when the input signal is transformed from the high logic level to the low logic level.

16 (original): The phase-frequency detector of claim 13, wherein the input signal is a wobble signal from an optical disc, and the target clock signal is a wobble clock signal corresponding to the wobble signal in the optical disc system.